

AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

- 1 **1.** (currently amended) A system for extending a signal path of a host bus
2 comprising:
3 a first repeater portion connected to a first segment of the host bus;
4 a second repeater portion connected to a second, non-hierarchical
5 segment of the host bus remote from the first portion of the host bus, where the
6 first and second portions of the repeater are connected by a serial link.

- 1 **2.** (original) The system according to claim 1, wherein the serial link is
2 chosen from one of the following: LVDS, Gigabit Ethernet, InfiniBand, IEEE1394,
3 RF Wireless, Infrared Wireless, or any combination of these.

- 1 **3.** (original) The system according to claim 2, wherein the host bus is a PCI
2 bus.

- 1 **4.** (original) The system according to claim 2, wherein the host bus is an
2 LPC (Low Pin Count) bus as defined by Intel 1997.

1 **5.** (original) The system according to claim **1**, wherein at least one of the
2 repeater portions further comprise:
3 an interface to the host bus segment;
4 a transaction queue with a data buffer connected to the interface;
5 a link translation layer connected the transaction queue to translate
6 incoming transactions from the host bus into serial streams to be sent over a
7 serial link.

1 **6.** (original) The system according to claim **3**, wherein at least one of the
2 repeater portions further comprise:
3 an interface to the host bus segment;
4 a transaction queue with a data buffer connected to the interface;
5 a link translation layer connected the transaction queue to translate
6 incoming transactions from the host bus into serial streams to be sent over a
7 serial link.

1 **7.** (original) The system according to claim **2**, wherein at least one of the
2 repeater portions further comprise:
3 an interface to the host bus segment;
4 a transaction queue with a data buffer connected to the interface;
5 a link translation layer connected the transaction queue to translate
6 incoming transactions from the host bus into serial streams to be sent over a
7 serial link.

1 **8.** (original) The system according to claim **5**, further comprising a
2 transaction decode circuit connected to the interface to the host bus segment to
3 determine which transactions on the host bus to accept and pass on over the
4 serial link.

1 **9.** (original) The system according to claim **6**, further comprising a
2 transaction decode circuit connected to the interface to the host bus segment to
3 determine which transactions on the host bus to accept and pass on over the
4 serial link.

1 **10.** (original) The system according to claim **7**, further comprising a
2 transaction decode circuit connected to the interface to the host bus segment to
3 determine which transactions on the host bus to accept and pass on over the
4 serial link.

Claims 11-14 (canceled).